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Kathy Manke
Avago Technologies Limited
4380 Ziegler Road
Fort Collins, CO 80525

| EXAMINER | |
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| LEE, CHUN KUAN | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

avagoip@system.foundationip.com
kathy.manke@avagotech.com
scott.weitzel@avagotech.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/721,606 | SUL ET AL. | |
| | Examiner | Art Unit | |
| | Chun-Kuan (Mike) Lee | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-7 and 12-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7 and 12-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

## RESPONSE TO ARGUMENTS

1. Applicant's arguments with respect to claims 2-7 and 12-26 have been considered but are moot in view of the new grounds of rejection. Rejection of claims 2 and 7 under 35 U.S.C. 112 second paragraph are withdrawn. Currently, claims 1 and 8-11 are canceled and claims 2-7 and 12-26 are pending for examination.

## I. INFORMATION CONCERNING OATH/DECLARATION

### *Oath/Declaration*

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

## II. INFORMATION CONCERNING DRAWINGS

### *Drawings*

3. The applicant's drawings submitted are acceptable for examination purposes.

## III. REJECTIONS BASED ON PRIOR ART

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 5-7 and 12-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Chennupati (US Patent 6,833,728) and Swami et al. (US Patent 7,154,299).

5. As per claim 2, AAPA teaches an integrated circuit comprising:

a plurality of pins (Drawings, Fig. 1, ref. 2, 12) including a input pin (Drawings, Fig. 1, ref. 2) and a output pin (Drawings, Fig. 1, ref. 12);

a scan path (Drawings, Fig. 1, ref. 9) having an input via the input pin and an output via the output pin (Drawings, Fig. 1); and

the scan path receiving input data for testing via the input pin and outputting the produced output data via the output pin (Specification, page 1, ll. 4-6).

AAPA does not teach the integrated circuit comprising:

an input/output (I/O) pin coupled to the input and the output of the scan path, wherein:

the pin inputs scan test data to the scan path at a first test time ...; and

the pin outputs scan test data from the scan path at a second test time.

Chennupati teaches a system and a method comprising a single bi-directional pin (Fig. 1, ref. 152) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25), therefore the bi-directional pin have a data path for receiving data and

another data path for output data (Fig. 1, ref. 156); wherein the data are clocked in and out of the bi-directional pin a different times (col. 1, ll. 15-17).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin into AAPA's pins for the benefit of reducing the number pins or allow additional pins to be used for other purposes (Chennupati, col. 5, ll. 34-37) to obtain the invention as specified in claim 2. The resulting combination of the references further teaches the integrated circuit further comprising:

the bi-directional pin is utilized for input and output of data, such that the bi-directional pin is coupled to the input and the output of the scan path:

wherein:

the bi-directional pin inputs data for testing to the scan path during the first period of time and outputs the produced output data from the scan path during the second period of time, as the inputting and the outputting of data are implemented at different period of times.

Swami teaches a system and a method of implementing a bi-directional input/output (I/O) pin responsive to an input enable control signal (col. 1, l. 65 to col. 2, l. 4 and col. 3, l. 57 to col. 4, l. 35).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Swami's enabling signals into AAPA and Chennupati's pins for the benefit of optimizing access of circuitry by implementing selective

connection and providing bi-direction access (Swami, col. 2, ll. 13-18) to obtain the invention as specified in claim 2.

6. As per claim 5, AAPA, Chennupati and Swami teach all the limitations of claim 2 as discussed above, where Chennupati further teaches the integrated circuit further comprising wherein the scan path comprises a series of scan paths (Chennupati, Fig. 2 and col. 5, ll. 38-44), wherein the first of the series of scan path is the path for the transferring of write data into the memory and the second of the series of scan path is the path for the outputting of the read data from the memory.

7. As per claim 6, AAPA, Chennupati and Swami teach all the limitations of claim 2 as discussed above, where Chennupati further teaches the integrated circuit further comprising functional circuitry (Chennupati, memory 204 of Fig. 2), wherein the scan path interacts with the functional circuitry (Chennupati, Fig. 2 and col. 5, ll. 38-44), wherein data are transferred to and from the memory through the scan path; and

8. As per claim 7, AAPA, Chennupati and Swami teach all the limitations of claim 2 as discussed above, where Chennupati and Swami further teach the integrated circuit further comprising functional circuitry (Chennupati, memory circuit of memory 204 of Fig. 2) wherein:

the I/O pin inputs functional test data (write data) to the functional circuitry (e.g. memory circuit of memory) at a third test time (Chennupati, Fig. 2 and col. 5, ll. 38-44),

as the subsequent write data is send through the L0 bus line to the first I/O pin of the memory following the second test time; and

the I/O pin outputs functional test data (read data) from the functional circuitry (e.g. memory circuit of memory) responsive to an output enable control signal at a fourth test time (Chennupati, Fig. 2 and col. 5, ll. 38-44 and Swami, col. 1, l. 65 to col. 2, l. 4 and col. 3, l. 57 to col. 4, l. 35), as the subsequent read data is outputted by the memory, to the L0 bus line, through the first I/O pin following the third test time.

9. As per claim 12, AAPA teaches an integrated circuit comprising:

a functional circuit (Drawings, Fig. 1, ref. 5) producing functional output (Specification, page 1, ll. 25-31);

a I/O pin (Drawings, Fig. 1, ref. 2) that acts as input at a first time (Specification, page 1, ll. 5-8);

an I/O circuitry comprising:

a virtual pin multiplexer (Drawings, Fig. 1, ref. 7) coupled to (1) the functional circuit (Drawings, Fig. 1, ref. 5) to received the functional output and (2) the scan path (Drawings, Fig. 1, ref. 9) to receive the scan output, the virtual pin multiplexer providing a virtual pin multiplexer output (Specification, p. 1, ll.18-22), wherein the virtual pin multiplexer output outputs to a output logic (Fig. 1, ref. 11); and

a D flip-flop (Fig 3, ref. 17) coupled to the (1) receiving of the scan output data (Fig. 3, ref. 8) and (2) outputting the data through the corresponding output (Fig. 3, ref.

18), wherein the D flip-flop holds the received data for a clock cycle (Specification, p. 2, ll. 20-26)

AAPA does not teach the integrated circuit comprising the I/O circuitry comprising:

the I/O pin acting as both input and output and having a respective scan path that produces scan output;

an input buffer ... coupled to (1) the I/O pin to receive an input signal and to (2) the functional circuit to provide the input signal;

a virtual pin output buffer ... to the I/O pin to provide output; and

a virtual pin flip-flop coupled to the (1) virtual pin multiplexer to receive the virtual pin multiplexer output and (2) the virtual pin output buffer to provide the virtual pin multiplexer output, the virtual pin flip-flop holding the received for a clock cycle.

Chennupati teaches a system and a method comprising:

a single bi-directional pin (Fig. 1, ref. 152) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25) and the data is inputted into a device (Fig. 1, ref. 150) through a respective INPUT2 data path and outputted from the device through a respective OUTPUT2 data path (Fig. 1, ref. 156), wherein the received INPUT2 data would have been processed by other components in the device to generated the OUTPUT2 data to be outputted (Fig. 1 and col. 4, ll. 27-29) wherein the data are clocked in and out of the bi-directional pin a different times (col. 1, ll. 15-17);

a input buffer (Fig. 1, ref. 164) coupled to the bi-directional pin (Fig. 1, ref. 152) to receive input data and to forward the data the circuitry within the device (Fig. 1, ref. 150) to provide the INPUT2 (Fig. 1); and

an output buffer (Fig. 1, ref. 154) coupled to the bi-directional pin (Fig. 1, ref. 152) to provide OUTPUT2 (Fig. 1).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin into AAPA's pins for the benefit of reducing the number pins or allow additional pins to be used for other purposes (Chennupati, col. 5, ll. 34-37) to obtain the invention as specified in claim 12. The resulting combination of the references further teaches the integrated circuit comprising:

the bi-directional pin (e.g. I/O pin) receiving input data during the first time and outputting data during the second time, the bi-directional pin having the respective scan path to produce the OUTPUT2 (e.g. scan output);

the I/O circuitry, comprising:

the input buffer coupled to the bi-directional pin to receive input data and to the functional circuit to provide the INPUT2;

the output buffer coupled to the bi-directional pin to provide the OUTPUT2;

the D flip-flop coupled to the output of the virtual pin multiplexer to receive the scan output data and to the output buffer for via the output for outputting of the data received from the virtual pin multiplexer, wherein the D flip-flop holds the received data for a clock cycle.

Swami teaches a system and a method of implementing a bi-directional input/output (I/O) pin responsive to an input enable control signal and responsive to a virtual pin enable (e.g. output enable) control signal (col. 1, l. 65 to col. 2, l. 4 and col. 3, l. 57 to col. 4, l. 35).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Swami's enabling signals into AAPA and Chennupati's pins for the benefit of optimizing access of circuitry by implementing selective connection and providing bi-direction access (Swami, col. 2, ll. 13-18) to obtain the invention as specified in claim 12.

10. As per claim 13, AAPA, Chennupati and Swami teach all the limitation of claim 12 as discussed above, where both further teach the integrated circuit further comprising:

a number of scan paths (Chennupati, Fig. 2 and col. 5, ll. 38-44) as each of the plurality of bus lines have the corresponding scan path resulting in four scan path;

the same number of I/O pins (Chennupati, Fig. 2 and col. 5, ll. 38-44) as there are four I/O pads connected to the corresponding bus line; and

the same number of I/O circuitry, wherein the same number of virtual pin of flip-flops (AAPA, Drawings, Fig. 2 and Fig. 3, ref. 17) form at least one register, as each of the I/O pad is coupled to the corresponding I/O circuitry with the D flip-flop, therefore the combined plurality of D flip-flops forms the at least one register.

11. As per claim 14, AAPA, Chennupati and Swami teach all the limitation of claim 13 as discussed above, where AAPA further teaches the integrated circuit further comprising:

each virtual pin flip flop (AAPA, Drawings, D flip-flop 17 of Fig. 3) comprising:

a compact-control signal (AAPA, Drawings, mask signal 13 of Fig. 3);

an output-data signal (AAPA, Drawings, scan output data (SOD) 8 of Fig. 3); and

an AND-gate (AAPA, Drawings, Fig. 3, ref. 15) receiving the compact-control signal (AAPA, Drawings, Fig. 3, ref. 13) and the output-data signal (AAPA, Drawings, Fig. 3, ref. 8) to eliminate the output of data with don't-care nature (AAPA, Specification, page 2, ll. 20-25), as the AND-gate is utilized to eliminate the output of data with don't-care nature; and

the register is a compaction register (AAPA, Drawings, Fig. 2, and Specification, page 2, ll. 1-5), as each of the I/O pads is operable for both inputting scan input data (SID) and outputting scan output data (SOD), therefore it would have been obvious to implement the compactor at the I/O pads for outputting and utilizing the register as compaction register.

12. As per claim 15, AAPA, Chennupati and Swami teach all the limitation of claim 13 as discussed above, where AAPA further teaches the integrated circuit comprising wherein each I/O circuitry further comprises:

a reseed multiplexer (AAPA, Drawings, Fig. 4, ref. 25) receiving the scan output data (AAPA, Drawings, scan output data 28 of Fig. 4) from the scan path and scan input (AAPA, Drawings, Fig. 4, ref. 23) derived from the input buffer, the reseed multiplexer obviously provides the scan output or the scan input to the virtual pin multiplexer (AAPA, Drawings, Fig. 1, ref. 7);

a reseed control signal controlling the reseed multiplexer (AAPA, Specification, page 2, l. 31 to page 3, l. 3), wherein the reseed multiplexer is multiplexing input data between the scan input data and the output of the XOR-gate (AAPA, Drawings, Fig. 4, ref. 29), therefore the reseed control signal is required to determine which of the input is to be outputted to the D flip-flop (AAPA, Drawings, Fig. 4, ref. 20); and

the register is a reseed register (AAPA, Specification, page 2, l. 27 to page 3, l. 3) as the register is utilized for reseeding.

13. As per claim 16, AAPA, Chennupati and Swami teach all the limitation of claim 13 as discussed above, where AAPA further teaches the integrated circuit comprising wherein:

each I/O circuitry further comprises

an XOR-gate (AAPA, Drawings, Fig. 4, ref. 29) coupled to receive a linear feedback shift register (LFSR) input (AAPA, Drawings, Fig. 4, ref. 27) and a LFSR

feedback (AAPA, Drawings, Fig. 4, ref. 28), the XOR-gate providing an XOR-gate output (Fig. 4 and Specification, page 3, ll. 1-3);

a reseed multiplexer (AAPA, Drawings, Fig. 4, ref. 25) coupled to receive (1) the XOR-gate output (AAPA, Drawings, output of XOR-gate 29 of Fig. 4) and (2) scan input (AAPA, Drawings, Fig. 4, ref. 23), the reseed multiplexer providing a reseed multiplexer output (Fig. 4);

a reseed flip-flop (AAPA, Drawings, Fig. 4, ref. 20) coupled to receive the reseed multiplexer output (i.e. from the reseed multiplexer 25 of Fig. 4, AAPA, Drawings), the reseed flip-flop providing a reseed flip-flop output (AAPA, Drawings, Fig. 4, ref. 26); and

a input multiplexer (AAPA, Drawings, Fig. 4, ref. 22) coupled to receive the input signal (AAPA, Drawings, Fig. 4, ref. 21) and the reseed flip-flop output (AAPA, Drawings, Fig. 4, ref. 26), the input multiplexer generating the scan input (AAPA, Drawings, Fig. 4, ref. 23).

14. As per claim 17, AAPA, Chennupati and Swami teach all the limitation of claim 13 as discussed above, where AAPA further teaches the integrated circuit comprising:

a second number of flip-flops (AAPA, Drawings, Fig. 3, ref. 17) that form a compaction register wherein:

the integrated circuit performs reseeding and compaction at the same time (AAPA, Specification, page 1, l. 29 to page 3, l. 3), wherein the reseeding and compaction are performed by the different number of flip-flops (AAPA, Drawings, Fig. 3, ref. 17 and Fig. 4, ref. 20).

15. As per claim 18, AAPA, Chennupati and Swami teach all the limitation of claim 17 as discussed above, where AAPA further teaches the integrated circuit comprising wherein the compaction register is read serially (AAPA, Specification, page 1, ll. 7-9), as shifting of data is implemented serially.

16. As per claim 19, AAPA teaches a method comprising:

inputting scan data to a first I/O pin (Drawings, Fig. 1, ref. 2) during a first time (Specification, page 1, ll. 5-8);

processing the scan data in a scan path to produce scan output data (Specification, page 1, ll. 8-9); and

outputting the scan output data to a second I/O pin (Drawings, Fig. 1, ref. 12) at a second time (Specification, page 1, ll. 5-8).

AAPA does not teach the method comprising wherein the input and the output of data ... are transferred over the same I/O pin as the scan data is processed in a respective scan path.

Chennupati teaches a system and a method comprising a single bi-directional pin (Fig. 1, ref. 152) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25), wherein input data to be processed is received through the respective INPUT2 data path, and after processing, output data is outputted through the respective OUTPUT2 data path (Fig. 1, ref. 156).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin into AAPA's pins for the benefit of reducing the number pins or allow additional pins to be used for other purposes (Chennupati, col. 5, ll. 34-37) to obtain the invention as specified in claim 19. The resulting combination of the references teaches the integrated circuit further comprising the bi-directional I/O pins for receiving scan data to be processed in the respective scan path, and after processing to obtain the scan output data, scan output data is output through said bi-directional I/O pins at the second time.

Swami teaches a system and a method of implementing a bi-directional input/output (I/O) pin responsive to an input enable control signal and a mode control signal, and responsive to an output enable control signal (col. 1, l. 65 to col. 2, l. 4 and col. 3, l. 57 to col. 4, l. 35).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Swami's enabling and mode signals into AAPA and Chennupati's pins for the benefit of optimizing access of circuitry by implementing selective connection and providing bi-direction access (Swami, col. 2, ll. 13-18) to obtain the invention as specified in claim 19.

17. As per claim 20, AAPA, Chennupati and Swami teach all the limitation of claim 19 as discussed above, where AAPA further teaches the method comprising:

multiplexing output data (AAPA, Drawings, Fig. 1, ref. 6) and scan output data (AAPA, Drawings, Fig. 1, ref. 10) by utilizing a multiplexer (Fig. 1, ref. 7); and

storing the output data or scan output data in a flip-flop (AAPA, Drawings, D flip-flop 17 of Fig. 3) during the first time, as data is buffered in the flop-flop before outputting during the second time.

18. As per claim 21, AAPA, Chennupati and Swami teach all the limitation of claim 20 as discussed above, where both further teach the method comprising:

connecting a number of flip-flops (AAPA, Drawings, D flip-flop 17 of Fig. 3 and D flip-flop 20 of Fig. 4) associated with I/O pins; and

forming a register (AAPA, Drawings, D flip-flop 20 of Fig. 4) for performing a reseed test (AAPA, Specification, page 2, l. 27 to page 3, l. 3 and Chennupati, Fig. 2), wherein there are four I/O pins and each is connected to the corresponding D flip-flop (AAPA, Drawings, Fig. 4, ref. 20) to form the register for implementing reseeding test.

19. As per claim 22, AAPA, Chennupati and Swami teach all the limitation of claim 21 as discussed above, where AAPA further teaches the method comprising wherein forming a register further comprises:

sending a compact control signal (AAPA, Drawings, mask signal 13 of Fig. 3);

AND-gating (AAPA, Drawings, AND-gate 15 of Fig. 3) the compact control signal with the output data (AAPA, Drawings, scan output data (SOD) 8 of Fig. 3);

eliminating don't care data (AAPA, Specification, page 2, ll. 14-26), wherein the AND-gate is utilized to eliminate the don't care data; and

performing compaction (AAPA, Drawings, Fig. 2-3).

20. As per claim 23, AAPA, Chennupati and Swami teach all the limitation of claim 21 as discussed above, where AAPA further teaches the method comprising wherein forming a register further comprises:

sending a reseed control signal to a reseed multiplexer (AAPA, Drawings, Fig. 4, ref. 25), wherein the reseed multiplexer is multiplexing between two inputs, therefore there must be the corresponding reseed control single controlling the reseed multiplexer to select between the two input signals;

multiplexing functional output data (AAPA, Drawings, Fig. 4, ref. 28) and scan input data (AAPA, Drawings, Fig. 4, ref. 23); and

performing the reseed test (AAPA, Specification, page 2, l. 27 to page 3, l. 3).

21. As per claim 24, AAPA, Chennupati and Swami teach all the limitation of claim 23 as discussed above, where AAPA further teaches the method comprising wherein multiplexing further comprises:

receiving gated input from a linear feedback shift register (AAPA, Drawings, Fig. 4, ref. 27) as the output from the linear feedback shift register is inputted into the XOR-gate, to be multiplexed by the reseed multiplexer; and

performing a linear feedback shift register reseed test (AAPA, Specification, page 2, l. 27 to page 3, l. 3), as the scan output data is feedback to the register.

22. As per claim 25, AAPA, Chennupati and Swami teach all the limitation of claim 19 as discussed above, where Chennupati further teaches the method comprising wherein the first time and the second time occur during the same clock cycle (Chennupati, col. 1, ll. 26-28), as the port can simultaneous transmit and receive input and output signal, therefore the inputting and the outputting of data can be implemented over the same clock cycle.

23. As per claim 26, AAPA, Chennupati and Swami teach all the limitation of claim 12 as discussed above, where Chennupati further teach the integrated circuit further comprising an output buffer (Chennupati, Fig. 1, ref. 154) coupled to (1) the functional circuit to received the functional output (Chennupati, Fig. 1, ref. OUTPUT2) and (2) the I/O pin (Chennupati, Fig. 1, ref. 152) to provide the function output (Chennupati, Fig. 1, ref. OUTPUT2).

24. Claim 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Chennupati (US Patent 6,833,728), Herzel (US Patent 6,271,732) and Swami et al. (US Patent 7,154,299).

25. As per claim 3, AAPA teaches an integrated circuit, comprising:

a scan path (Drawings, Fig. 1, ref. 9);

inputting scan test to an input of the scan path via a inputting pin (Drawings, Fig. 1, ref. 2) (Specification, p. 1, ll. 4-12); and

outputting scan test data from the scan path via a outputting pin (Drawings, Fig. 1, ref. 12) (Specification, p. 1, ll. 4-12).

AAPA does not teach the integrated circuit, comprising

two separate scan path;

a first I/O pin inputting input scan test to an input of the first scan path at a first test time and outputting output scan test data from an output of the second scan path at a second test time ...; and

a second I/O pin inputting input scan test to an input of the second scan path at a first test time and outputting output scan test data from an output of the first scan path at a second test time ....

Chennupati teaches a system and a method comprising

a plurality of single bi-directional pin (Fig. 1, ref. 152 and Fig. 2) is utilized for both inputting and outputting of data (col. 1, ll. 15-17 and col. 4, ll. 23-25), therefore the bi-directional pin have a data path for receiving data (Fig. 1, ref. 164) and another data path for output data (Fig. 1, ref. 156); wherein the data are clocked in and out of the bi-directional pin a different times (col. 1, ll. 15-17);

a first bi-directional pin (e.g. pin coupled to line L0 of Fig. 2) inputting data into the memory (Fig. 2, ref. 204) at during a first period of time (e.g. WRITE 0 of Fig. 2) and

outputting data from memory (Fig. 2, ref. 204) during a second period of time (e.g. READ 0 of Fig. 2), as data are clocked in and out of the bi-directional pin a different times; and

a second bi-directional pin (e.g. pin coupled to line L1 of Fig. 2) inputting data into the memory (Fig. 2, ref. 204) at during the first period of time (e.g. WRITE 1 of Fig. 2) and outputting data from memory (Fig. 2, ref. 204) during the second period of time (e.g. READ 1 of Fig. 2), as data are clocked in and out of the bi-directional pin a different times.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Chennupati's bi-directional pin into AAPA's pins for the benefit of reducing the number pins or allow additional pins to be used for other purposes (Chennupati, col. 5, ll. 34-37) to obtain the invention as specified in claim 3. The resulting combination of the references further teaches the integrated circuit, comprising:

the first scan path coupled between the input and the out of the first bi-directional pin, as the scan test data is inputted into the first scan path during the first period of time and outputted from the first scan path during the second period of time; and

the second scan path coupled between the input and the out of the second bi-directional pin, as the scan test data is inputted into the second scan path during the first period of time and outputted from the second scan path during the second period of time.

Herzel teaches an integrated circuit comprising:

a first circuit component (Fig. 1, ref. 10a);

wherein the first circuit component's upper input (Fig. 1, ref. 10a input "+") which is located on the upper data path would be outputted by the first circuit component's lower output (Fig. 1, ref. 10b output "+") which is located on the lower data path; and

wherein the first circuit component's lower input (Fig. 1, ref. 10a input "-") which is located on the lower data path would be outputted by the first circuit component's upper output (Fig. 1, ref. 10b output "-") which is located on the upper data path.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Herzel's circuitry into AAPA and Chennupati's integrated circuit for the benefit of enabling the testing of various types of circuits, including Herzel's circuit component to obtain the invention as specified in claim 3. The resulting combination of the references further teaches the integrated circuit comprising.

the first bi-directional pin receiving the scan test data into the first scan path during the first period of time and outputting from the second scan path during the second period of time; and

the second bi-directional pin inputting the scan test data into the second scan path during the first period of time and outputting from the first scan path during the second period of time.

Swami teaches a system and a method of implementing a bi-directional input/output (I/O) pin responsive to a first and second input enable control signal (col. 1, l. 65 to col. 2, l. 4 and col. 3, l. 57 to col. 4, l. 35).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Swami's enabling signals into AAPA, Chennupati and Herzel's pins for the benefit of optimizing access of circuitry by implementing selective connection and providing bi-direction access (Swami, col. 2, ll. 13-18) to obtain the invention as specified in claim 3.

26. As per claim 4, AAPA, Chennupati, Herzel and Swami teach all the limitations of claim 3 as discussed above, where Chennupati further teaches the integrated circuit comprising wherein at least one of the first scan path and the second scan path further comprises a series of scan paths (Chennupati, Fig. 2 and col. 5, ll. 38-44), wherein the first of the series of scan path is the path for the transferring of write data into the memory and the second of the series of scan path is the path for the outputting of the read data from the memory.

## IV. CLOSING COMMENTS

### *Conclusion*

### a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

#### a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, applicant's amendments necessitated the new grounds of rejection presented in this Office action; therefore, claims 2-8 and 12-26 have received a final action on the merits. Please See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**b. DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

## IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 25, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER